HIGH SPEED TURBO CODES DECODER FOR 3G USING PIPELINED SISO LOG-MAP DECODERS ARCHITECTURE

Abstract of Disclosure

The invention encompasses several improved Turbo codes method to provide a more practical and simpler method for implementation a Turbo Codes Decoder in ASIC or DSP coding. (1) Two pipelined Log-MAP decoders are used for iterative decoding of received data. (2) Output data from the first decoder A are stored in the Interleaver RAM memory, and the second decoder B stores output data in the De-interleaver RAM memory, such that in pipeline mode Decoder A decodes data from the De-interleaver RAM memory while the Decoder B decodes data from the De-interleaver RAM memory at the same time. (3) Log-MAP decoders are simpler to implement in ASIC with only Adder circuits, and are low-power consumption. (4) Pipelined Log-MAP decoders method provide high speed data throughput.

Figures